MμL 9033

16-BIT MEMORY CELL

MEMORY MICROLOGIC® INTEGRATED CIRCUITS

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The MμL 9033 is a Planar* epitaxial integrated 16-bit, bit-oriented, non-destructive readout memory cell, compatible with Fairchild Transistor-Transistor Micrologic® (TTμL) and other Compatible Current-Sinking Logic (CCSL) integrated circuits. This memory cell, organized as 16 word by one bit, is designed for high-speed scratch-pad memory applications.

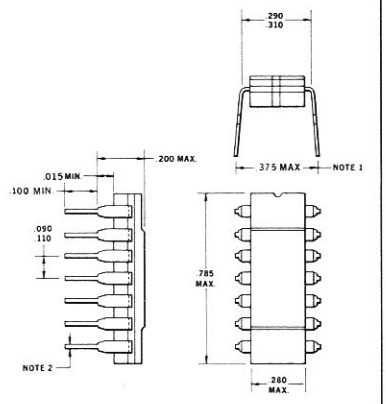
OPERATION — The memory cell consists of 16 R-S flip-flops arranged in an addressable four-by-four matrix. The desired bit location is selected by raising the coincident X-Y address lines to a logic "1" (typically 3.5 volts) and holding the non-selected address lines at logic "0" (approximately ground). As many as four locations may be addressed simultaneously without destroying stored information. The data and complemented data stored at the addressed bit location may be read at the output terminals. If the addressed bit location contains a "1", the one output (S_1) will be in a low state; zero output (S_0) will be in a high state.

Writing is accomplished by activating one of the write amplifiers. To write a "1", the desired bit location is addressed and the input of the "write one" (W_1) amplifier is raised to a logic "1". To write a "0", the input of the "write zero" (W_0) amplifier is raised to a logic "1".

The outputs are open-collector, which may be wire "OR" ed for word expansion. An external resistor should be returned to V_{CC} to pull-up the wire "OR"ed outputs.

TYPICAL DUAL IN-LINE PACKAGE

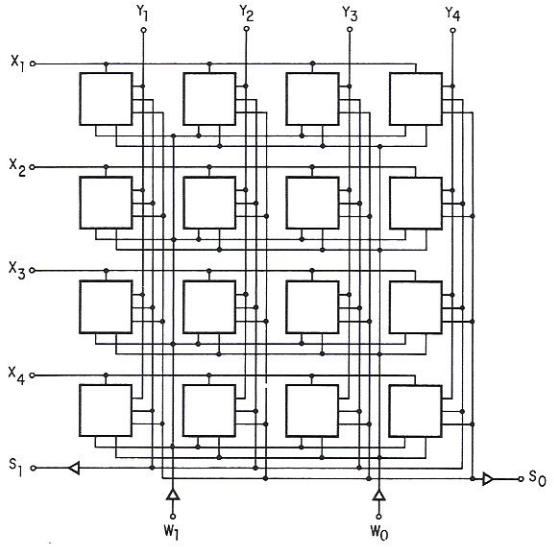
(In accordance with JEDEC TO—116)

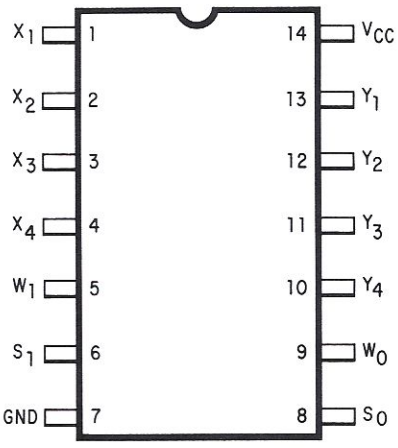


NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

ORDER PART NO: A6A903359X
X = 1 FOR 40 mA FAN-OUT
X = 2 FOR 20 mA FAN-OUT

LOGIC DIAGRAM AND PIN ARRANGEMENTS





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X,Y– ADDRESS
W – WRITE INPUT
S – SENSE OUTPUT

*Planar is a patented Fairchild process.

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FAIRCHILD SEMICONDUCTOR
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RATINGS

SYMBOL	PARAMETER	LIMITS MIN.	TYP.	MAX.	UNITS
V_{CC}	Supply Voltage			7.0	Volts
V_{CC}	Operating Supply Voltage	4.5	5.0	5.5	Volts
	Input Voltage			5.5	Volts
	Output Voltage			5.5	Volts
T_A	Ambient Temperature	0		+75	°C
T_S	Storage Temperature	−65		+150	°C
θ_{J-A}	Thermal Resistance, Junction-to-Ambient:				
	(1) Free Air		120		°C/Watt
	(2) 200 Ft./Min. Air Flow		65		°C/Watt
	(3) 400 Ft./Min. Air Flow		55		°C/Watt
θ_{J-C}	Thermal Resistance, Junction-to-Case		30		°C/Watt
P_D	Power Dissipation		0.25		Watts

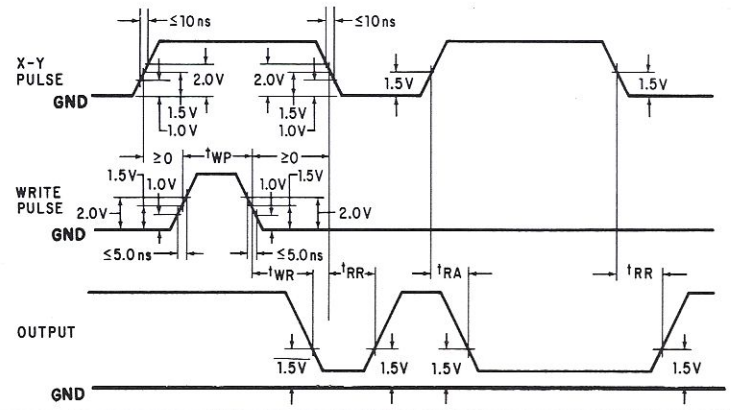
D. C. CHARACTERISTICS ($V_{CC} = 5.0$ V, $T_A = 0°C$ to $+75°C$)

TEST	DESCRIPTION	CONDITIONS	LIMITS MIN.	MAX.	UNITS
I_{FA}	Address Input Low Current	$V_{FA} = 0$ V		11	mA
I_{RA}	Address Input High Current	$V_{RA} = 4.5$ V		0.4	mA
I_{FW}	Write Input Low Current	$V_{FW} = 0$ V		1.5	mA
I_{RW}	Write Input High Current	$V_{FR} = 4.5$ V		0.1	mA
V_{IL}	Input Low Voltage			1.0	Volts
V_{IH}	Input High Voltage		2.1		Volts
V_{OL}	Output Low Voltage 9033591	$R_L = 120\ \Omega$ to V_{CC}		0.45	Volts
	9033592	$R_L = 240\ \Omega$ to V_{CC}		0.45	Volts
I_{OH}	Output Leakage Current	$V_{OH} = V_{CC}$		0.1	mA
I_{CC}	Power Drain	$V_{CC} = 5.25$ V Inputs Grounded		65	mA

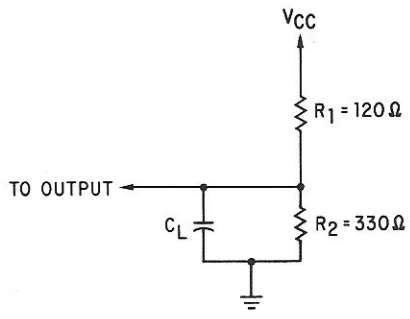
SWITCHING TIME TESTS ($V_{CC} = 5.0$ V, $T_A = 0°C$ to $+75°C$)

TEST	DESCRIPTION	CONDITIONS	C_L (pF)	LIMITS MIN.	MAX.	UNITS
t_{WP}	Write Pulse Width	One X-Y location high, all others low, W_0 low when checking W_1, W_1 low when checking W_0.		25		ns
t_{WR}	Write Recovery Time	One X-Y location high, all others low, "1" previously stored when testing S_0, "0" previously stored when checking S_1.	30		35	ns
t_{RR}	Read Recovery Time	One X-Y location switched, all others low, "1" previously stored when testing S_1, "0"	30		20	ns
t_{RA}	Read Access Time	previously stored when testing S_0.	200		30	ns
t_{RA}	Read Access Time	Four X-Y locations switched, all others low, "1"s previously stored when testing S_1, "0"s previously stored when testing S_0.	30		22	ns

SWITCHING TEST WAVEFORMS



SWITCHING TEST OUTPUT LOAD



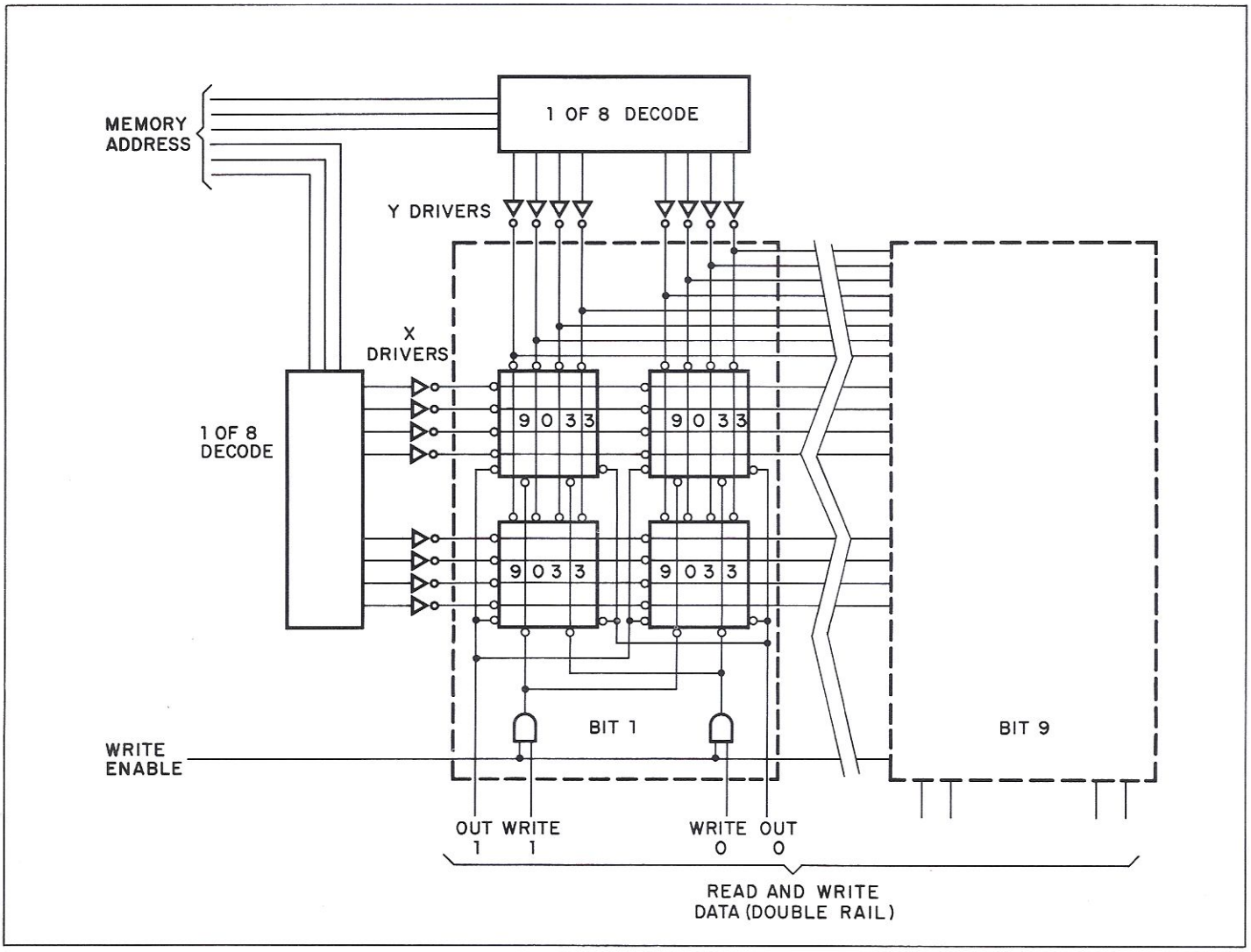
APPLICATIONS

A memory utilizing 9033 16-bit memory cells may have any desired word length and the number of words in the memory is a multiple of 16. To illustrate how the 9033 may be used to construct a larger memory, the following example is given:

The six memory address lines from an external source may be decoded at the first level with two 1-out-of-8 decoders. Each output of the 1-out-of-8 decoders controls a driving transistor. These driving transistors provide the current necessary to drive eight X and eight Y address lines. Each transistor drives 18 9033 memory cells. The figure below shows the organization of such a memory. The four 9033's shown in detail represent 64 words of one bit each. There are nine such groups of four 9033's each, each group representing one of the nine bit positions. The 16 address driving transistors drive all nine groups.

The 1-out-of-8 decoder produces one of the eight combinations of three inputs only if the Enable input is at a high logic level. If the Enable input is at a high logic level, one, and only one, of the eight outputs assumes a low logic level. If the Enable input is at a low logic level, all the outputs assume a high logic level. This feature allows the several decoders to be used for memory addressing where the number of words is increased to say 128 or 256.

The example given above is only one of many organizations and is presented as an illustration. Obviously many address decoding schemes may be utilized depending on memory size, driver fan-out, decoder fan-out, wiring, heat dissipation, etc.



FAIRCHILD MEMORY MICROLOGIC® INTEGRATED CIRCUIT MμL 9033

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